**SECOND SEMESTER 2022-23**

**COURSE HANDOUT**

**Date: 09.01.2024**

*Course No* : **CS F342**

*Course Title* : **Computer Architecture**

*Instructors incharge* : S Gurunarayanan

*Instructor (Lab)* : Aalelai Vendhan

**1. Scope and Objective:**

This course aims at introducing the concept of computer architecture and organization. It involves design aspects, and deals with the current trends in computing architecture. System resources such as memory technology and I/O subsystems needed to achieve proportional increase in performance will also be discussed.

2. **Learning outcomes:**

* Understand various architectural techniques used in implementation of complex logic functions
* Apply these techniques in building different computing architectures
* Analyze different performance metrics of different computing architectures
* Design associated systems resources to achieve proportional increase in performance.

**3. Text Book:**

(T1) Patterson, David A & J L Hennessy, *Computer Organization& Design*, Elsevier, 6th Ed., 2021.

(T2) Samir Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, Pearson Education Asia, 2nd Ed. 2006.

**4. Reference Books:**

1. J.L. Hennessy & D.A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kauffmann, 6th Ed, 2019.

**5. Course Plan:**

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| --- | --- | --- | --- |
| Lecture No. | Topics to be covered | Learning Outcomes | Reference to T1 |
| 01 | Introduction | Overview of the course | Ch. 1.1-1.3. |
| 02 | Introduction to Performance metrics of computing architectures | Definition different parameters impacting processor Performance | Ch. 1.5-1.10 |
| 03, 04 | MIPS Architecture & Instruction Set  Overview of different classes and formats of MIPS instruction set | Overview of different classes of instructions and addressing modes of a select RISC Processor. | Ch. 2 |
| 05-06 | Computer Arithmetic: Building hardware structures | Understanding the design and implementation of different arithmetic and logic blocks | Ch. 3.1 – 3.5 |
| 07,08,09 | Data path Design: Building using functional blocks | Single Cycle & Multicycle Datapath Implementation of MIPS Processor | Ch. 4.1 – 4.4 |
| 10,11 | Control Hardware: FSM based Design | Controller Design of a Multicycle Implementation of MIPS Processor | Appendix – D |
| 12,13 | Exceptions & Microprogramming | Ch. 4.9 |
| 14,15 | Floating Point Arithmetic: Hardware Architectures | Understanding floating point algebra and its hardware implementation | Ch 3.6 – 3.10 |
| 16 | Role of Performance |  | Ch. 1.4 |
| 17, 18 | Memory organization- Introduction | Role of Memory in a Processor based Cache Memory Design techniques | Ch5.1 |
| 19, 20 | Cache Memory Organization: Mapping Schemes | Ch.5.2 |
| 21, 22, 23 | Cache Performance | Ch. 5.3 |
| 24, 25,26 | Pipelining – Design Issues | Designing a Pipelines Processor and understanding the associated hazards and methods to handle them effectively. | Ch. 4.5 – 4.6 |
| 27,28 | Data Hazards | Ch. 4.7 |
| 29,30 | Control Hazards | Ch. 4.8 |
| 31, 32 | Static Branch Prediction | Class notes |
| 33,34,35 | Dynamic Branch Prediction | Class notes |
| 36,37 | I/O Organization |  | Ch. 6 |
| 38-40 | Advanced Concepts in pipelining | Concept of Instruction Level Parallelism and its impact in Processor Performance | Ch. 4.12 |

**6. Evaluation Scheme:**

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| --- | --- | --- | --- | --- | --- |
| **EC No.** | **Evaluation Component** | **Duration (Min)** | **Maximum marks** | Date & Time | Remarks |
| 1 | Mid Semester Test | 90 | 60 | 14/03 - 2.00 - 3.30PM | Closed Book |
| 2 | Lab/Assignments \*\* | ----- | 60 | Will be announced | Open Book |
| 3 | Comprehensive examination | 180 | 80 | 15/05 FN | Open Book/Closed Book |

\*\* Details will be announced in the class & on course web page. Text book **T2** will be used for Lab Assignments. (A Detailed Instruction sheet and plan for Laboratory sessions will be shared separately)

**7. Chamber Consultation Hours:** Mon: 4PM to 5 PM

**8. Notices:** Notices regarding the course will be put up on the CMS.

**9.Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

**Instructor - in - charge**

**CS F342**